We claim:

1. In a circuit configuration for signal balancing in antiphase bus drivers for a bus having two driver paths, the bus drivers having a driver amplifier unit and an output stage driven by the driver amplifier unit in each of the driver paths, the output stage having a power transistor circuit for transmitting an antiphase signal via a two-wire line, and a control circuit configured to control a turn-on resistance of the power transistor circuits such that the power transistor circuits have a same turn-on resistance in the two driver paths, wherein the improvement comprises:

the control circuit being connected to precisely one of the driver paths and controlling the turn-on resistance of the power transistor circuit in the respective driver path.

2. The circuit configuration according to claim 1, wherein the bus with the two driver paths is a CAN bus.

3. The circuit configuration according to claim 1, wherein the power transistor circuit in a first driver path has a PMOS power transistor, and a second driver path has a DMOS power transistor.

4. The circuit configuration according to claim 3, wherein said control circuit is connected to control the turn-on resistance of the DMOS power transistor.

5. The circuit configuration according to claim 4, wherein said control circuit is configured to control the turn-on resistance by controlling a gate voltage for the DMOS power transistor.

6. The circuit configuration according to claim 3, wherein said control circuit is configured to control a gate voltage for the DMOS power transistor by controlling a supply voltage for the driver amplifier unit driving the DMOS power transistor.

7. The circuit configuration according to claim 1, wherein said control circuit comprises an internal antiphase bus driver representing a simulation of the bus driver to be balanced, said internal antiphase bus driver having components with a same degree of scaling as the bus driver to be balanced, and said internal bus driver having an internal pickup node carrying a center voltage.

8. The circuit configuration according to claim 1, wherein said control circuit has a sample and hold circuit, and, in a steady on-state of the bus driver to be balanced, said sample

and hold circuit measures and stores a center voltage of the bus driver.

9. A circuit configuration for signal balancing in an antiphase bus driver, which comprises:

first and second driver amplifier units respectively connected in each driver path of a bus carrying an antiphase signal on a two-wire line;

an output stage for outputting the antiphase signal, said output stage having power transistor circuits respectively driven by said first and second driver amplifier units; and

a control circuit connected only to one of said first and second driver amplifier units for controlling a turn-on resistance of said power transistor circuits and for setting the power transistor circuits in the two driver paths to have a mutually corresponding turn-on resistance.

10. The circuit configuration according to claim 9, wherein the bus with the two driver paths is a CAN bus.

11. The circuit configuration according to claim 9, wherein the power transistor circuit in one driver path has a PMOS power transistor, and the other driver path has a DMOS power transistor.

12. The circuit configuration according to claim 11, wherein said control circuit is connected to control the turn-on resistance of the DMOS power transistor.

13. The circuit configuration according to claim 12, wherein said control circuit is configured to control the turn-on resistance by controlling a gate voltage for the DMOS power transistor.

14. The circuit configuration according to claim 11, wherein said control circuit is configured to control a gate voltage for the DMOS power transistor by controlling a supply voltage for the driver amplifier unit driving the DMOS power transistor.

15. The circuit configuration according to claim 9, wherein said control circuit comprises an internal antiphase bus driver representing a simulation of the bus driver to be balanced, said internal antiphase bus driver having components with a same degree of scaling as the bus driver to be balanced, and said internal bus driver having an internal pickup node carrying a center voltage.

16. The circuit configuration according to claim 9, wherein said control circuit has a sample and hold circuit, and, in a

steady on-state of the bus driver to be balanced, said sample and hold circuit measures and stores a center voltage of the bus driver.